

L Number	Hits	Search Text	DB	Time stamp
15	5494	partition\$3 same rout\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/20 00:16
16	322	(partition\$3 same rout\$3) and diagonal	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/19 23:44
17	274	((partition\$3 same rout\$3) and diagonal) and stor\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/20 00:16
18	67	((partition\$3 same rout\$3) and diagonal) and stor\$3) and 716/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/19 23:45
19	191	((partition\$3 same rout\$3) and diagonal) and (region or sub-region)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/20 00:16
20	55	((partition\$3 same rout\$3) and diagonal) and (region or sub-region)) and 716/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/19 23:45
21	360	(partition\$3 same rout\$3) and 716/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/20 00:16
22	307	((partition\$3 same rout\$3) and 716/\$.ccls.) and stor\$3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/20 00:16
23	178	((partition\$3 same rout\$3) and 716/\$.ccls.) and stor\$3) and (region or sub-region)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/09/20 00:17

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030121015 A1	20030626	74	Method and apparatus for measuring congestion in a partitioned region	716/7
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20030115566 A1	20030619	118	Method and apparatus for pre-computing routes	716/14
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030115564 A1	20030619	80	Block based design methodology	716/8
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20030101428 A1	20030529	118	Routing method and apparatus	716/14
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20030088845 A1	20030508	115	Probabilistic routing method and apparatus	716/14
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20030088844 A1	20030508	118	Method and apparatus for pre-computing routes	716/14
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030088841 A1	20030508	50	Partitioning placement method and apparatus	716/8
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20030079193 A1	20030424	118	Routing method and apparatus that use diagonal routes	716/7
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20030066045 A1	20030403	118	Method and apparatus for identifying routes for nets	716/14
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20030066044 A1	20030403	118	Method and apparatus for identifying propagation for routes with diagonal edges	716/14
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20030066043 A1	20030403	117	Routing method and apparatus	716/13
12	<input type="checkbox"/>	<input type="checkbox"/>	US 20030066042 A1	20030403	118	ROUTING METHOD AND APPARATUS	716/13
13	<input type="checkbox"/>	<input type="checkbox"/>	US 20030056187 A1	20030320	118	METHOD AND APPARTUS FOR ROUTING	716/14
14	<input type="checkbox"/>	<input type="checkbox"/>	US 20030023943 A1	20030130	118	Method and apparatus for producing sub-optimal routes for a net by generating fake configurations	716/7
15	<input type="checkbox"/>	<input type="checkbox"/>	US 20030018947 A1	20030123	118	Hierarchical routing method and apparatus that use diagonal routes	716/7

	U	1	Document ID	Issue Date	Pages	Title	Current OR
16	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20030005398 A1	20030102	33	TIMING-DRIVEN GLOBAL PLACEMENT BASED ON GEOMETRY-AWARE TIMING BUDGETS	716/8
17	<input type="checkbox"/>	<input type="checkbox"/>	US 20020199165 A1	20021226	118	Method and apparatus for pre-computing attributes of routes	716/14
18	<input type="checkbox"/>	<input type="checkbox"/>	US 20020174412 A1	20021121	118	Method and apparatus for pre-computing routes for multiple wiring models	716/12
19	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020170027 A1	20021114	56	Method and apparatus for pre-computing placement costs	716/10
20	<input type="checkbox"/>	<input type="checkbox"/>	US 20020166105 A1	20021107	118	"LP method and apparatus for identifying routes"	716/14
21	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020166098 A1	20021107	80	Block based design methodology	716/1
22	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020157075 A1	20021024	56	Method and apparatus for computing placement costs	716/10
23	<input type="checkbox"/>	<input type="checkbox"/>	US 20020147958 A1	20021010	117	Method and apparatus for adaptively selecting the wiring model for a design region	716/12
24	<input type="checkbox"/>	<input type="checkbox"/>	US 20020133798 A1	20020919	44	Method and apparatus for considering diagonal wiring in placement	716/10
25	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020124231 A1	20020905	61	Method and apparatus for pre-computing and using placement costs within a partitioned region for multiple wiring models	716/7
26	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020100007 A1	20020725	64	Recursive partitioning placement method and apparatus	716/7
27	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020073390 A1	20020613	44	Method and apparatus for using a diagonal line to measure an attribute of a bounding box of a net	716/8
28	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020073380 A1	20020613	89	Block based design methodology with programmable components	716/1
29	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020069397 A1	20020606	56	Method and apparatus for placing circuit modules	716/12

	U	1	Document ID	Issue Date	Pages	Title	Current OR
30	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20020016952 A1	20020207	81	Block based design methodology	716/18
31	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20010056570 A1	20011227	34	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	716/16
32	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20010042237 A1	20011115	80	Block based design methodology	716/8
33	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20010039641 A1	20011108	80	Block based design methodology	716/8
34	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20010025369 A1	20010927	78	Block based design methodology	716/18
35	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20010018756 A1	20010830	81	Block based design methodology	716/1
36	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 20010016933 A1	20010823	80	Block based design methodology	716/1
37	<input type="checkbox"/>	<input type="checkbox"/>	US 6618849 B2	20030909	113	Method and apparatus for identifying routes for nets	716/12
38	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6594800 B2	20030715	71	Block based design methodology	716/1
39	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6574778 B2	20030603	70	Block based design methodology	716/1
40	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6567957 B1	20030520	71	Block based design methodology	716/4
41	<input type="checkbox"/>	<input type="checkbox"/>	US 6526559 B2	20030225	31	Method for creating circuit redundancy in programmable logic devices	716/16

	U	1	Document ID	Issue Date	Pages	Title	Current OR
42	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6526558 B2	20030225	36	Methods for configuring FPGA's having variable grain blocks and shared logic for providing symmetric routing of result output to differently-directed and tristateable interconnect resources	716/16
43	<input type="checkbox"/>	<input type="checkbox"/>	US 6516455 B1	20030204	48	Partitioning placement method using diagonal cutlines	716/7
44	<input type="checkbox"/>	<input type="checkbox"/>	US 6480991 B1	20021112	30	Timing-driven global placement based on geometry-aware timing budgets	716/8
45	<input type="checkbox"/>	<input type="checkbox"/>	US 6473891 B1	20021029	13	Wire routing to control skew	716/12
46	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6269467 B1	20010731	71	Block based design methodology	716/1
47	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5822214 A	19981013	135	CAD for hexagonal architecture	716/10
48	<input type="checkbox"/>	<input type="checkbox"/>	US 5640327 A	19970617	29	Apparatus and method for partitioning resources for interconnections	716/7
49	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5617322 A	19970401	23	Mesh generator and generating method	700/98
50	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5587922 A	19961224	12	Multidimensional spectral load balancing	716/2
51	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5528508 A	19960618	79	System and method for verifying a hierarchical circuit design	716/8
52	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5519628 A	19960521	78	System and method for formulating subsets of a hierarchical circuit design	716/10

	U	1	Document ID	Issue Date	Pages	Title	Current OR
53	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5497334 A	19960305	78	Application generator for use in verifying a hierarchical circuit design	716/5
54	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5481473 A	19960102	78	System and method for building interconnections in a hierarchical circuit design	716/5
55	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5448493 A	19950905	30	Structure and method for manually controlling automatic configuration in an integrated circuit logic block array	716/7